

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. 2885/96	Serial No. 10/551,891
	Applicant(s) VORBACH	
	Filing Date August 28, 2006	Group Art Unit 2183

**U.S. PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,173,419	01-09-2001	Barnett			
	6,668,237	12-23-2003	Guccione et al.			
	6,836,842	12-28-2004	Guccione et al.			

**FOREIGN PATENT DOCUMENTS**

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

**OTHER DOCUMENTS**

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Ballagh et al., "Java Debug Hardware Models Using JBits," 8 <sup>th</sup> Reconfigurable Architectures Workshop, 2001, 8 pages.
	Bellows et al., "Designing Run-Time Reconfigurable Systems with JHDL," Journal of VLSI Signal Processing, Vol. 28, Kluwer Academic Publishers, The Netherlands, 2001, pp. 29-45.
	Guccione et al., "JBits: Java based interface for reconfigurable computing," Xilinx, Inc., San Jose, CA, 1999, 9 pages.
	Price et al., "Debug of Reconfigurable Systems," Xilinx, Inc., San Jose, CA, Proceedings of SPIE, 2000, pp. 181-187.
	Sundararajan et al., "Testing FPGA Devices Using JBits," Proc. MAPLD 2001, Maryland, USA, Katz (ed.), NASA, CA, 8 pages.
EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	